DATA SHEET

SA56600-42
System reset for lithium battery backup

Product data
Supersedes data of 2001 Apr 24
File under Integrated Circuits, Standard Analog

2001 Jun 19

Philips
Semiconductors

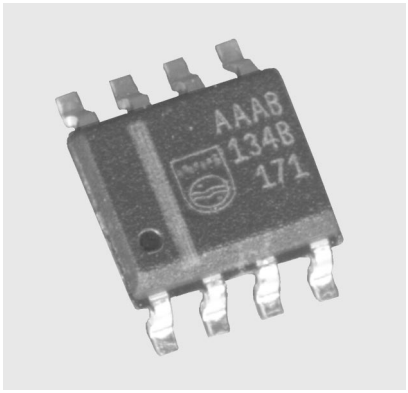
PHILIPS

System reset for lithium battery back-up SA56600-42

GENERAL DESCRIPTION

The SA56600-42 is designed to protect SRAM data in computer systems during periods of sagging power supply voltages and power outages. When the power supply voltage drops to typically 4.2 V, the CS output goes to a logic LOW state pulling CE to a LOW state, disabling the SRAM device. In addition, a reset logic LOW is asserted for system use. If the supply voltage drops further, to 3.3 V typically or lower, the SA56600-42 switches the system's operation from the main power supply source to the Lithium back-up battery. As the main supply is restored and the voltage rises to 3.3 V or higher, the SRAM support voltage transfers from the Lithium back-up battery to the main supply. When the main supply voltage rises to greater than typically 4.2 V, the CS output goes to a logic HIGH state for SRAM CE control. Reset assertion is released and normal operation is resumed. This sequence ensures reliable preservation of SRAM data during periods of supply deficiency and interruptions.

The SA56600-42 is offered in the SO8 surface mount package.



FEATURES

- Supply switching at 4.2 V_{DC} threshold (falling supply)
- $\overline{\text{RESET}}$ output
- Both CS and $\overline{\text{CS}}$ outputs available for SRAM control
- During battery back-up operation:
  - Low supply current (0.3 μA typical)
  - Low input/output voltage drop (0.3 V typical at 100 μA)
  - Low reverse current leakage (0.1 μA max.)
- During normal operation:
  - Low input/output voltage drop (0.2 V typical at 50 mA)
  - 4.8 V typical output voltage at 50 mA with V_{CC} = 5.0 V
  - Restoration of main supply operation at 3.3 V

APPLICATIONS

- Memory cards (SRAM)
- PCs, word processors
- FAX machines, photocopiers, office equipment
- Sequence controllers
- Video games and other equipment with SRAM

SIMPLIFIED SYSTEM DIAGRAM

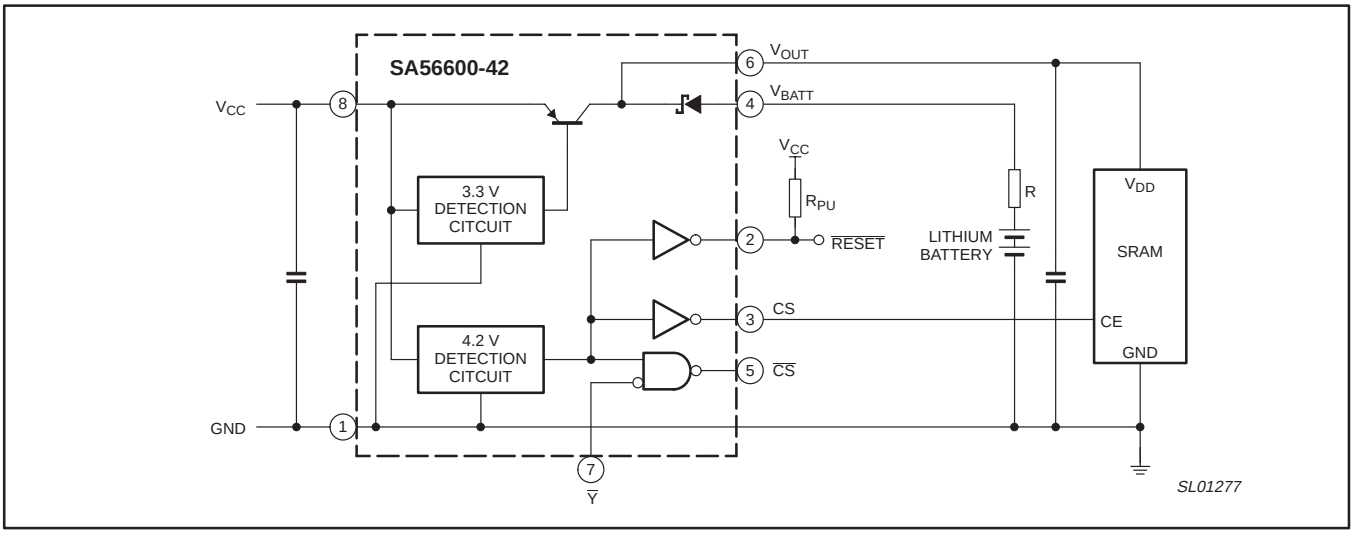


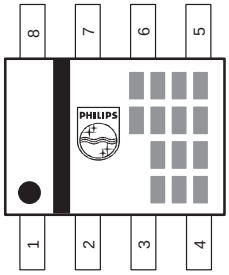
Figure 1. Simplified system diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
SA56600-42D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	–40 to +85 °C

Part number marking

The package is marked with a four letter code in the first line to the right of the logo. The first three letters designate the product. The fourth letter, represented by 'x', is a date tracking code. The remaining two or three lines of characters are internal manufacturing codes.



Part number	Marking
SA56600-42	A A A x

PIN CONFIGURATION

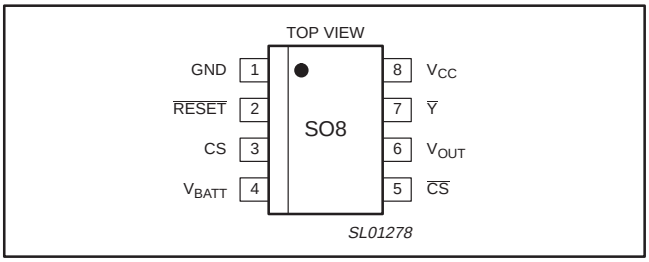


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	Circuit ground for the device.
2	$\overline{RESET}$	Asserted open collector output LOW whenever the V_{CC} input source voltage falls below V_S (4.2 V typical). The open collector topology requires an external pull-up resistor.
3	CS	Chip select HIGH output signal, asserted whenever the V_{CC} input source voltage is above V_S (4.2 V typical). Can be used as a chip enable HIGH (CE) signal for system SRAM.
4	V_{BATT}	Positive polarity connection for lithium back-up battery.
5	$\overline{CS}$	Asserted chip select LOW output signal whenever the V_{CC} input source voltage is above V_S (4.2 V typical) and $\overline{Y}$ is grounded. Can be used as a chip enable LOW ($\overline{CE}$) signal for system SRAM.
6	V_{OUT}	Primary power with lithium battery back-up power for the protected system. Switch over to lithium battery back-up operation occurs when V_{CC} falls below V_S.
7	$\overline{Y}$	Open Emitter input to microcontroller used to enable $\overline{CS}$ output (microcontroller controls $\overline{CS}$ function).
8	V_{CC}	Primary input power source for device.

MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC(max)}$	Power supply voltage	–0.3 to +7.0	V
$V_{CC(op)}$	Operating voltage	–0.3 to +7.0	V
I_O (V_{CC})	Output current	80	mA
I_O (V_{BATT})	Output current	200	µA
T_{oper}	Operating temperature	–40 to +85	°C
T_{stg}	Storage temperature	–40 to +125	°C
P	Power dissipation	250	mW

ELECTRICAL CHARACTERISTICS

Characteristics measured with V_{CC} = 5.0 V, and T_{amb} = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CC}	Supply current	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; I_O = 0 mA	–	1.4	2.2	mA
V_{SAT1}	I/O voltage difference 1	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; I_O = 1.0 mA	–	0.03	0.05	V
V_{O1}	Output voltage 1	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; I_O = 1.0 mA	4.95	4.97	–	V
V_{O2}	Output voltage 2	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; I_O = 15 mA	4.75	4.90	–	V
V_S	Detection threshold	V_{CC} falling	4.00	4.20	4.40	V
ΔV_S	Detection hysteresis	$\Delta V_S = V_{SH}$ (rising V_{CC}) – V_{SL} (falling V_{CC})	–	100	–	mA
V_{RSL}	Reset output LOW	V_{CC} = 3.7 V	–	0.2	0.4	V
I_{RSH}	Reset leakage current HIGH	V_{CC} = 5.0 V; V_{RS} = 7.0 V	–	±0.01	±0.1	µA
V_{OPL}	Reset assertion (minimum operating voltage)	$V_{RSL} \leq$ 0.4 V; V_{CC} falling; R_{PU} = 10 kΩ	–	0.8	1.2	V
V_{CSL}	CS output voltage LOW	V_{CC} = 3.7 V; V_{BATT} = 3.0 V; I_{CS} = 1.0 µA	–	–	0.1	V
V_{CSH}	CS output voltage HIGH	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; I_{CS} = –1.0 µA	4.90	–	–	V
$V_{\overline{CSL}}$	$\overline{CS}$ output voltage LOW	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; I_{CS} = 1.0 µA	–	–	0.2	V
$V_{\overline{CSH}}$	$\overline{CS}$ output voltage HIGH	V_{CC} = 3.7 V; V_{BATT} = 3.0 V; I_{CS} = –1.0 µA	V_O – 0.1	–	–	V
$\Delta V_S/\Delta T$	Detection voltage temperature characteristic	$-40 \leq T_{amb} \leq +85$	–	–	±0.05	%/°C
V_{BT}	Battery back-up threshold	V_{CC} falling	3.15	3.30	3.45	V
$V_{BT(HYS)}$	Battery back-up hysteresis	$V_{BT(HYS)}$ = V_{BTH} (V_{CC} rising) – V_{BTL} (V_{CC} falling)	–	100	1.0	mV
$V_{BT}/\Delta T$	Switching voltage temperature characteristic	$-40 \leq T_{amb} \leq +85$	–	–	±0.05	%/°C
I_L	Loss current	V_{CC} = 0 V; V_{BATT} = 3.0 V; I_O = 0 µA	–	0.3	0.5	µA
V_{SAT2}	I/O voltage difference 2	V_{CC} = 0 V; V_{BATT} = 3.0 V; I_O = 1.0 µA	–	0.2	0.3	V
V_{O3}	Output voltage 3	V_{CC} = 0 V; V_{BATT} = 3.0 V; I_O = 1.0 µA	2.7	2.8	–	V
V_{O4}	Output voltage 4	V_{CC} = 0 V; V_{BATT} = 3.0 V; I_{CS} = 100 µA	2.6	2.7	–	V
V_{REF}	Reference voltage (typical)		–	1.25	–	V
I_{BL}	V_{BATT} leakage current	V_{CC} = 5.0 V; V_{BATT} = 0 V	–	–	0.1	µA
I_{YLO}	$\overline{Y}$ current	V_{CC} = 5.0 V; V_{BATT} = 3.0 V; $V_{\overline{Y}}$ = 0 V	–	150	400	µA
t_{PLH}	$\overline{Y}$ propagation delay time (Note 1)	$V\overline{Y}$ = logic LOW to logic HIGH	–	8.0	20	ns
t_{PHL}	$\overline{Y}$ propagation delay time (Note 1)	$V\overline{Y}$ = logic HIGH to logic LOW	–	8.0	20	ns

NOTE:

1. $\overline{Y}$ input rise and fall time less than 6.0 ns. 15 pF capacitance load on $\overline{CS}$ (Pin 5 to GND).

TYPICAL PERFORMANCE CURVES

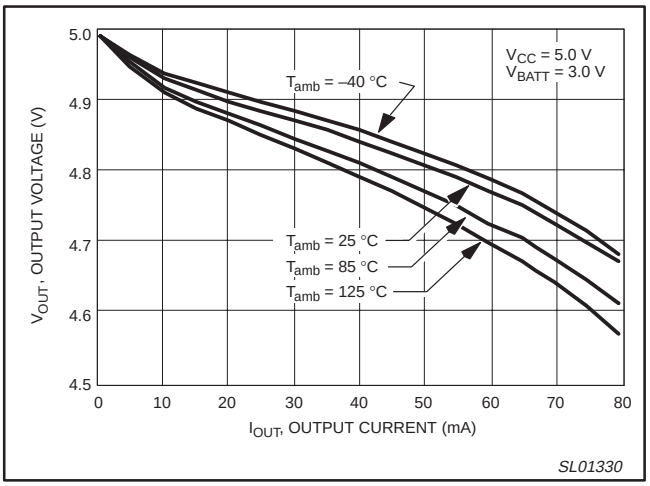


Figure 3. Output voltage versus output current.

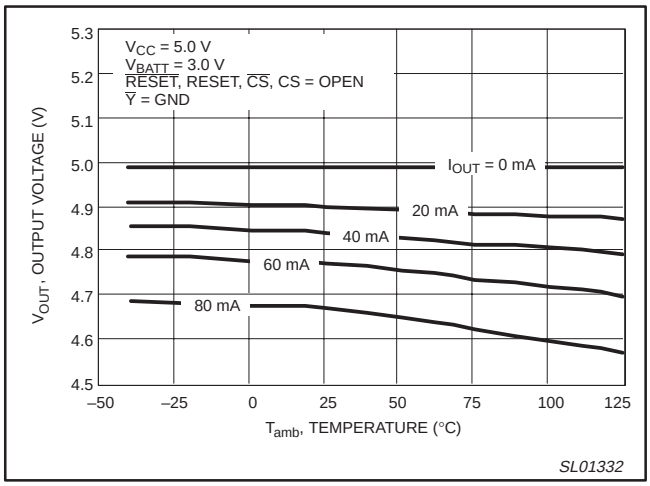


Figure 4. Output voltage versus temperature.

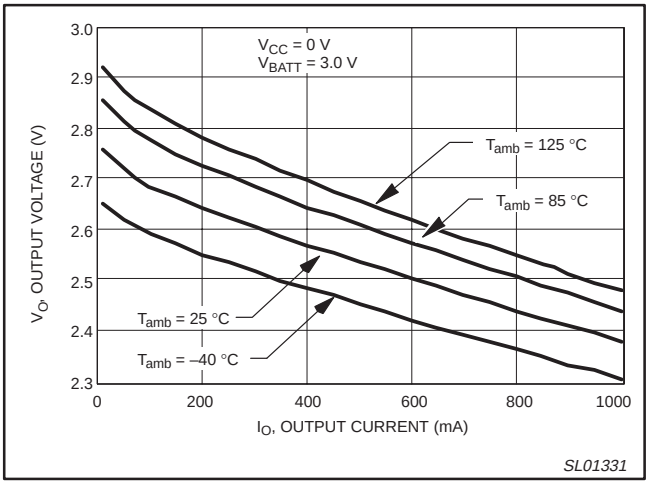


Figure 5. Output voltage versus current.

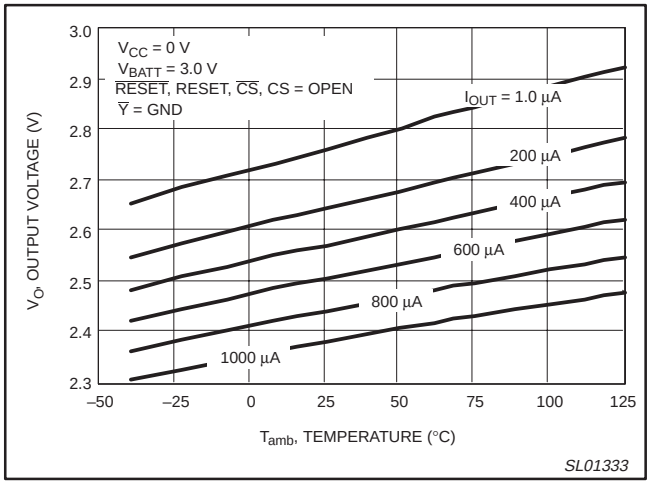


Figure 6. Output voltage versus temperature.

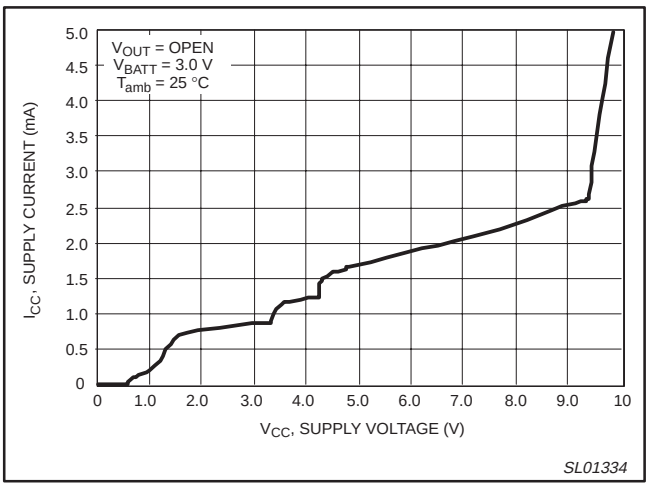


Figure 7. Supply current versus supply voltage.

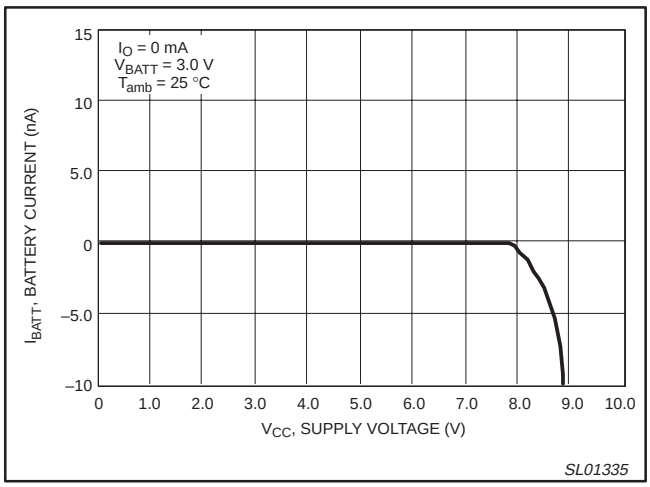


Figure 8. Battery current versus supply voltage.

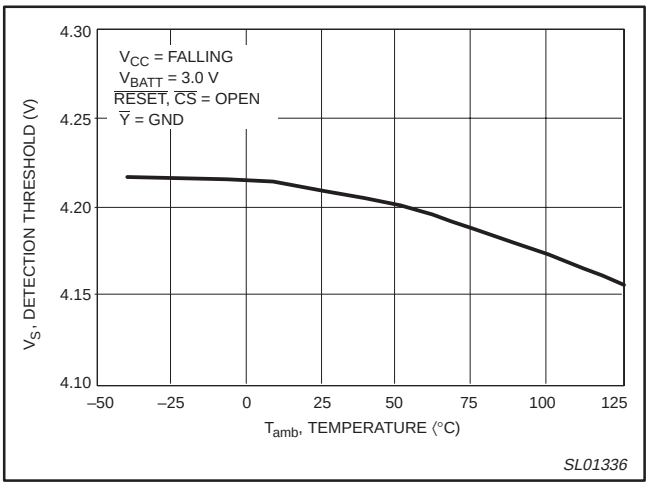


Figure 9. Detection threshold versus temperature.

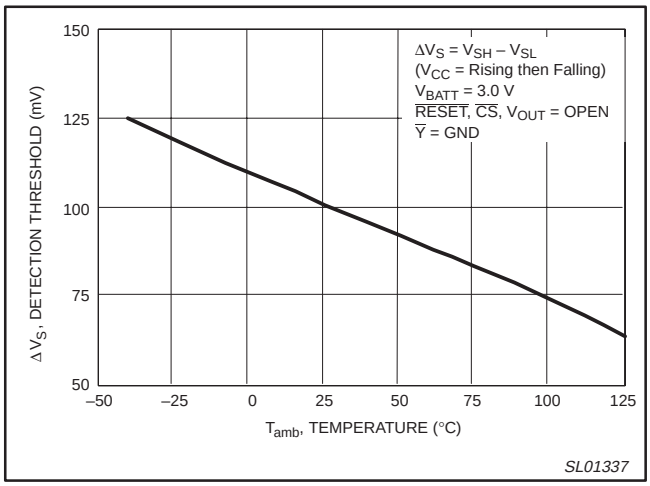


Figure 10. Detection hysteresis versus temperature.

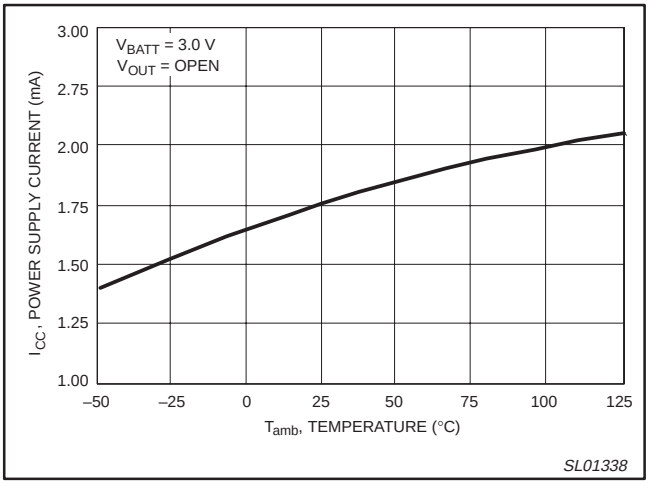


Figure 11. Power supply current versus temperature.

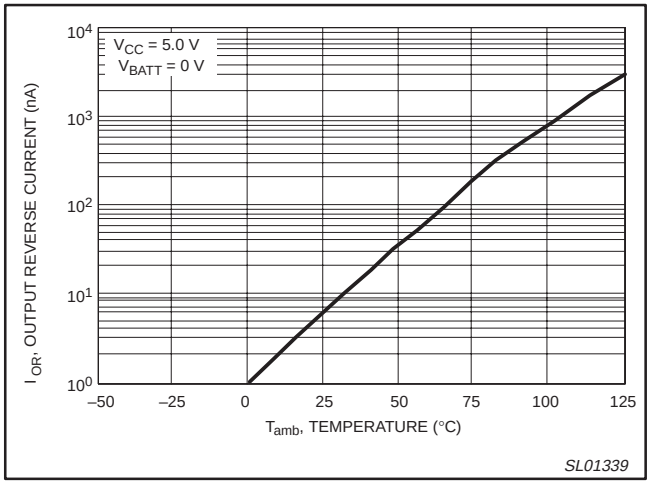


Figure 12. Output reverse current versus temperature.

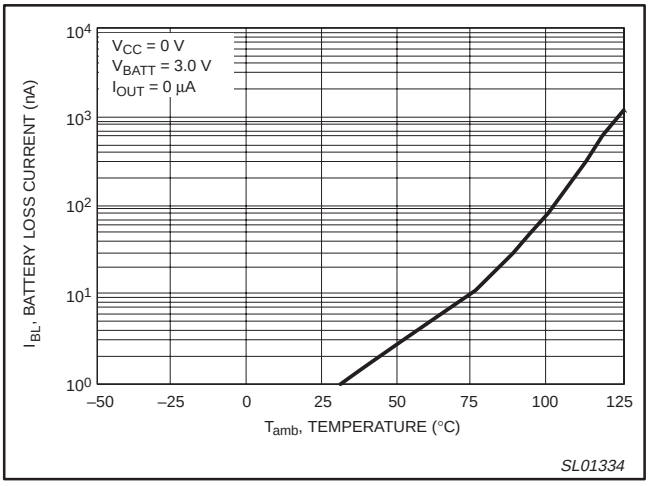


Figure 13. Battery loss current versus temperature.

TECHNICAL DESCRIPTION

The SA56600-42 provides battery back-up functions to protect SRAM data in computer memory systems. In addition, it provides RESET, Chip Select HIGH (CS), and Chip Select LOW ($\overline{CS}$) outputs. The device incorporates a 3.3 V detection circuit, 4.2 V detection circuit, PNP switching transistor, and Schottky diode for low drop lithium battery connection to the output.

During power-up, $\overline{RESET}$ is actively asserted (LOW logic state) at V_{CC} voltages as low as 0.8 V and does not output a release (HIGH logic state) until V_{CC} attains 4.2 V plus hysteresis. CS, in a similar manner, only transitions to a HIGH logic state when V_{CC} attains 4.2 V plus hysteresis. This ensures adequate voltage being present at the output of the SA56600 for proper operation of the associated computer system.

If the V_{CC} voltage falls below 4.2 V, CS and $\overline{RESET}$ both go to a LOW logic state. During this time, with CS in a LOW logic state, no data ca be read from, or written to, the SRAM device. If the primary voltage (V_{CC}) continues to fall to 3.3 V and below, the PNP switching transistor disconnects the primary input source power (V_{CC}) from the output and the Schottky diode automatically couples the lithium battery power to the output of the SA56600 to supply sustaining power to the SRAM memory.

The SA56600 provides complementary CS and $\overline{CS}$ outputs. The outputs differ in ways other than being simple complements of each other. The logic state of CS is strictly a function of V_{CC} voltage. When V_{CC} is above 4.2 V plus hysteresis, CS is in a HIGH logic state. When V_{CC} is below 4.2 V, CS is in a LOW logic state.

$\overline{CS}$ goes to a LOW logic state only when V_{CC} is above 4.2 V plus hysteresis, and $\overline{Y}$ is simultaneously at a LOW logic state. If $\overline{Y}$ is not a LOW logic state (is open or at a HIGH logic state) $\overline{CS}$ will be at a HIGH logic state. Essentially, $\overline{Y}$ functions as a control switch for $\overline{CS}$ and is normally used as an input gating signal from the computer's microprocessor.

Caution should be exercised in the application to keep the voltage on $\overline{Y}$ to less than 5.0 V when the V_{CC} voltage is less than 4.2 V to avoid breaking down the Emitter-Base junction of the internal NPN transistor associated with $\overline{Y}$. Breakdown of the junction may produce excessive current flow causing damage to the device. When the V_{CC} voltage is less than 4.2 V, the base of the NPN transistor associated with the $\overline{Y}$ is at a LOW logic state and most susceptible to an overvoltage on $\overline{Y}$.

Recovering primary V_{CC} power is sensed by the 3.3 V detection circuit. The PNP switching transistor is activated when the applied V_{CC} voltage reaches 3.3 V plus hysteresis. When this event occurs, the Schottky diode becomes back-biased, automatically disconnecting the lithium battery from the output and the SRAM is once again supported by the primary V_{CC} power source. Full operation is restored when the applied primary V_{CC} voltage reaches the required 4.2 V plus hysteresis value. This level is sensed by the 4.2 V detection circuit. $\overline{RESET}$ and CS are then caused to go to a HIGH logic state, and the computer memory is back in full operation without any loss of SRAM data.

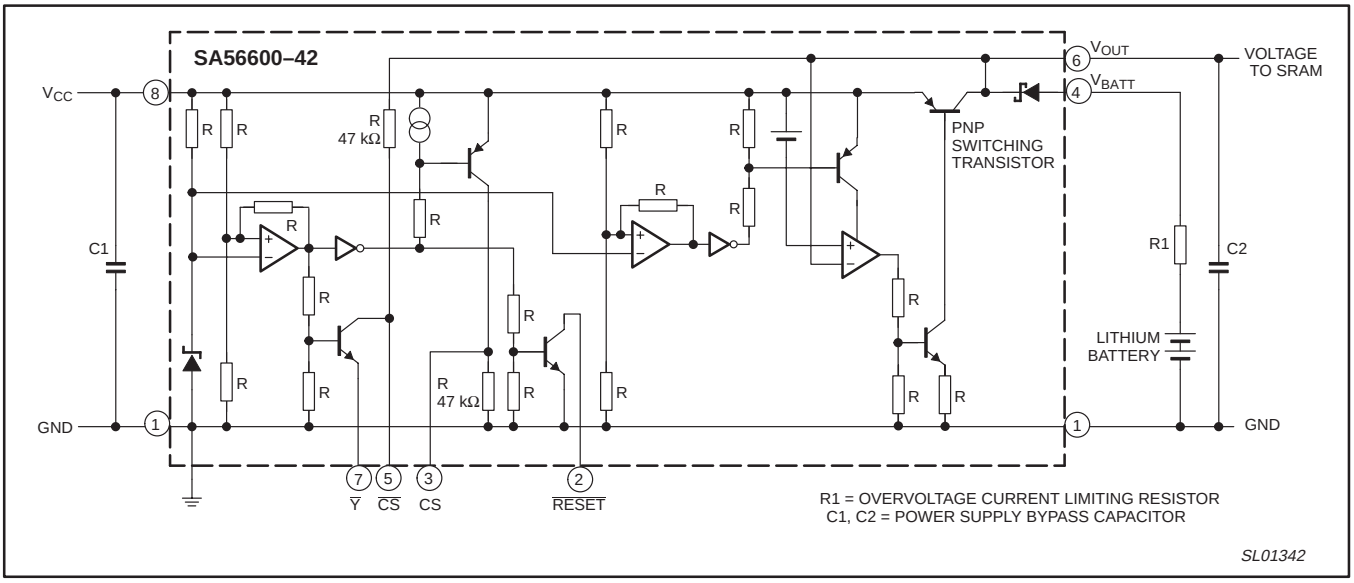


Figure 14. Functional diagram.

Timing diagram

The Timing Diagram shown in Figure 15 depicts the operation of the SA56600-42 in its intended application, with a 3.0 V Lithium battery serving as a backup power source for external SRAM circuitry (see the Simplified system diagram, Figure 1). Letters indicate events along the Time axis.

A: At 'A', the V_{CC} primary power source is off. As a result of the backup battery, the $\overline{CS}$ and V_{OUT} outputs are almost up to the Lithium battery potential (V_B). All other outputs ($\overline{Y}$, $\overline{RESET}$, and CS) are at or very near ground potential.

B - C: At 'B', the V_{CC} voltage begins to rise. Also the $\overline{RESET}$ voltage initially rises but then abruptly returns to a LOW state at 'C'. when the V_{CC} voltage reaches the level which activates the internal bias circuitry and asserts $\overline{RESET}$ to a logic LOW. This occurs at approximately 0.8 volts.

D - E: At 'D' the internal 3.3 V detection circuit is activated when V_{CC} voltage rises to 3.3 V. The circuit causes the PNP series pass switching transistor in the output to activate, connecting the main power supply voltage (V_{CC}) to the output. This causes the Lithium battery to be automatically disconnected from V_{OUT} by back-biasing the Schottky diode. As a result, $\overline{CS}$ and V_{OUT} begin to rise with V_{CC}.

E: At 'E', V_{CC} has risen to the upper detection threshold (V_S plus hysteresis) as sensed by the device's internal 4.2 V detection circuit. This event signals that the output voltage is adequate to support full operation of the associated external computer circuitry. $\overline{RESET}$ goes HIGH, allowing the microprocessor circuitry to operate. Simultaneously, CS also goes HIGH, signaling the SRAM to start receiving data. $\overline{CS}$ goes LOW as a result of $\overline{Y}$ simultaneously being at a LOW state.

$\overline{Y}$ controls the $\overline{CS}$ output. As long as $\overline{Y}$ is LOW, the $\overline{CS}$ output is enabled.

F: As V_{CC} continues to rise, $\overline{RESET}$, CS, and V_{OUT} also continue to rise. Just before 'F', $\overline{Y}$ is asserted HIGH by the microprocessing circuitry. This causes $\overline{CS}$ to change from a LOW state to a HIGH state. Following 'F' the microprocessing circuitry is signaling $\overline{Y}$ through repetitive cycles. This causes $\overline{CS}$ to also cycle, but has no effect on the battery circuit.

G: At 'G', the V_{CC} voltage begins to fall. As a result $\overline{RESET}$, CS, and V_{CC} fall.

H: When the V_{CC} voltage falls to V_S (4.2 V) it is detected by the internal 4.2 V detector circuit. The detector circuit forces $\overline{RESET}$ and CS LOW, deselecting the SRAM and stopping data storage and retrieval. The PNP series pass switching transistor disconnects the primary input source voltage from the output, transferring the SRAM to the backup battery. In addition, because $\overline{Y}$ is already at a LOW state, $\overline{CS}$ rises abruptly close to V_S followed by a continued fall to V_B (Lithium battery potential), following V_{CC}.

J: At 'J', V_{OUT} has also fallen with V_{CC} to a level that is now dictated by the Lithium battery potential. The Lithium battery is now maintaining the V_{OUT} voltage to preserve the SRAM data.

K - L: As the V_{CC} voltage falls to a level which no longer allows the internal bias circuitry to remain active, the assertion of $\overline{RESET}$ can no longer be maintained. $\overline{RESET}$ rises slightly, then falls to ground as V_{CC} falls to ground.

M: $\overline{Y}$ is asserted HIGH again by the microprocessor, but because V_{CC} is below V_S, $\overline{CS}$ remains HIGH and CS remains LOW, preventing the SRAM from being selected.

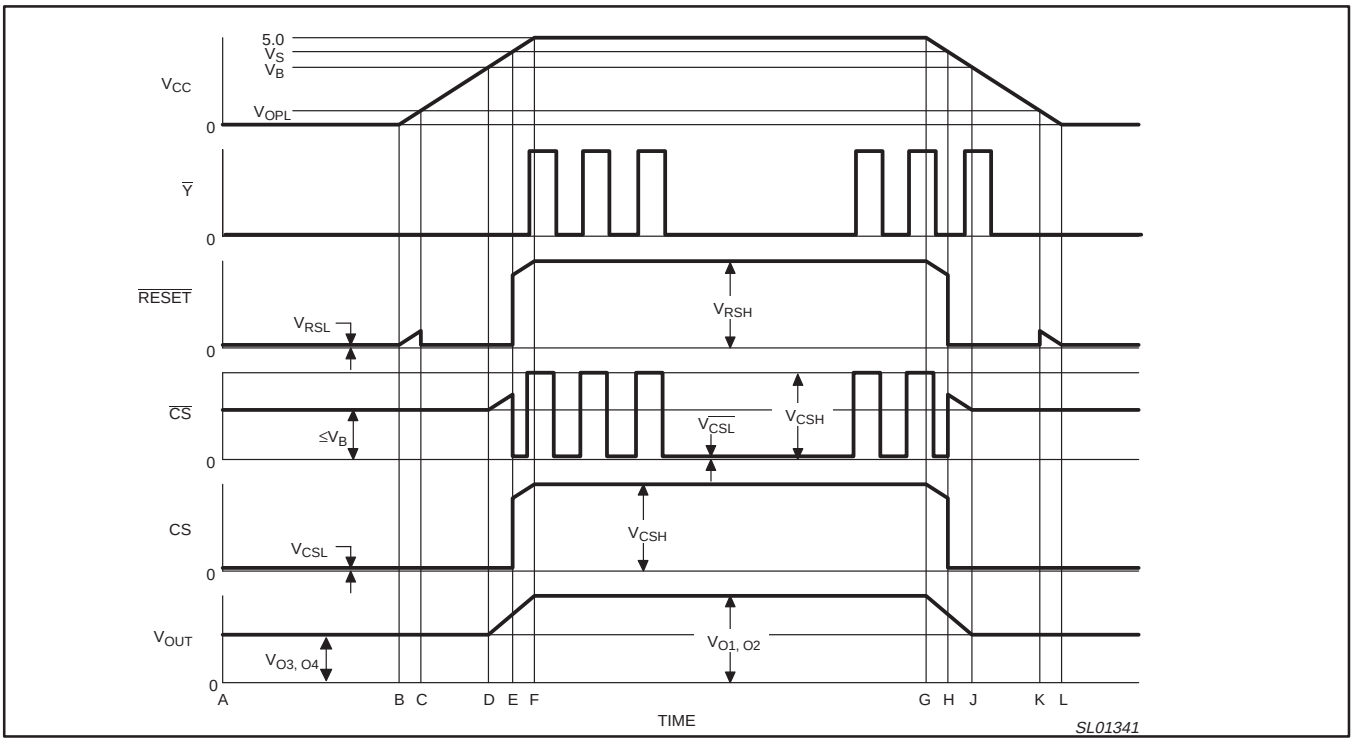


Figure 15. Timing diagram.

PACKING METHOD

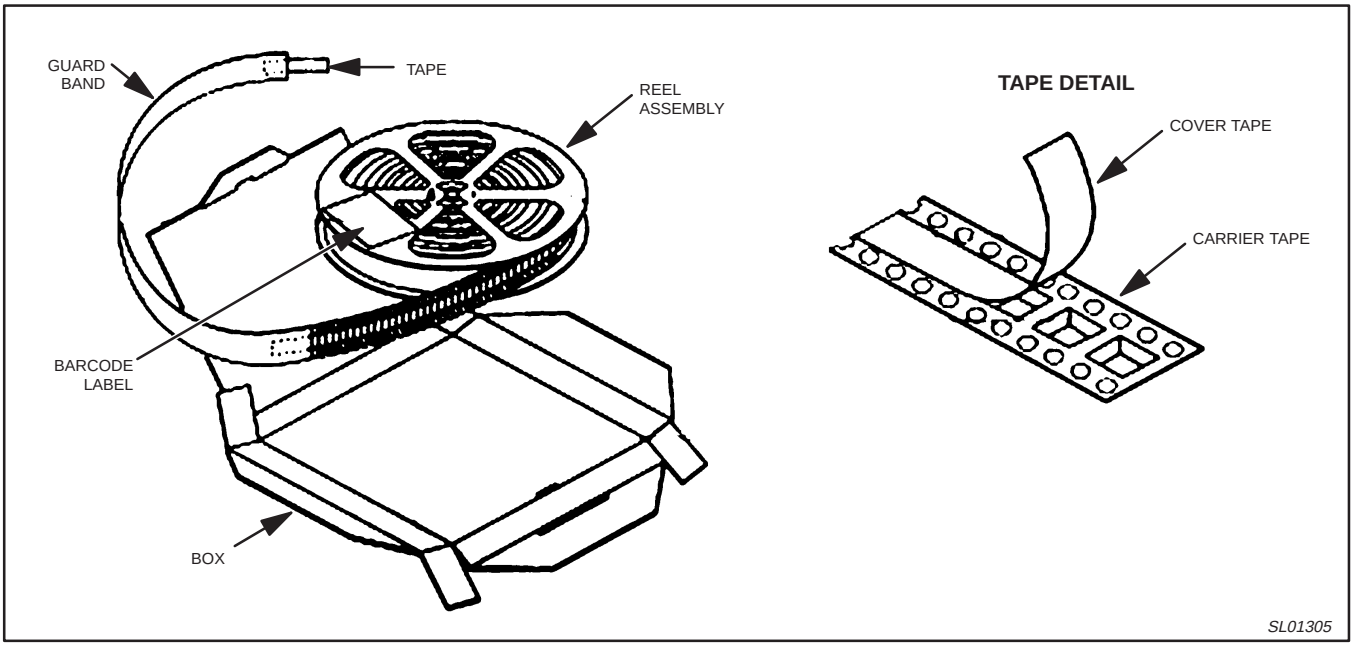
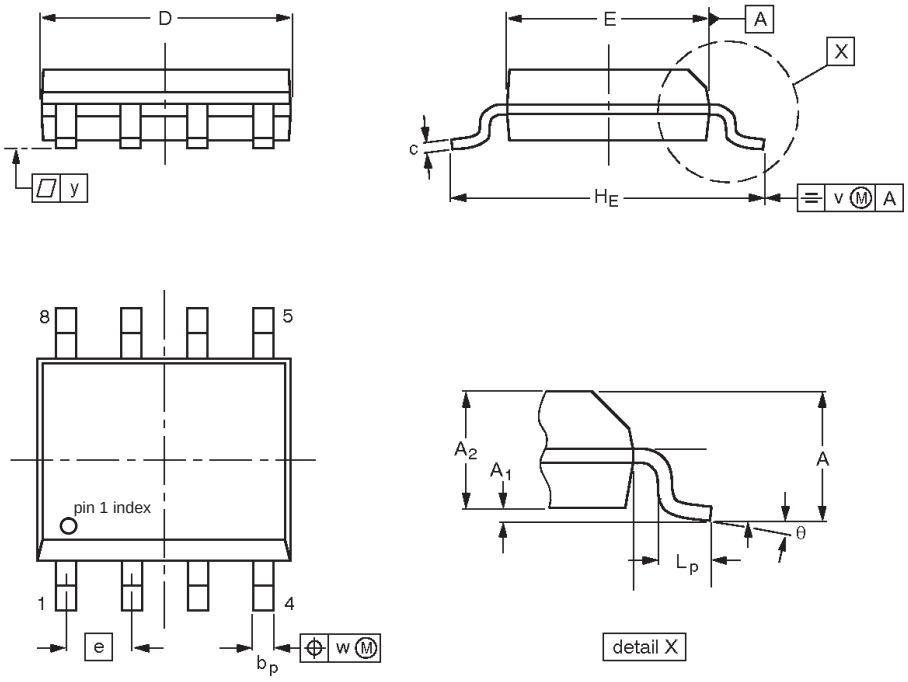
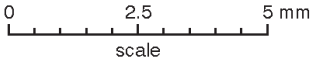


Figure 16. Tape and reel packing method.

SO8: plastic small outline package; 8 leads; body width 3.9 mm





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	B_2	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E		L_p				y		θ
mm	1.73	0.25 0.10	1.45 1.25	4.95 4.80	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8		1.27 0.38				0.076		8^o 0^o
inches	0.068	0.010 0.004	0.057 0.049	0.189 0.195	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228		0.050 0.015				0.003		

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			
	IEC	JEDEC	EIAJ	
SO8	076E03	MS-012		

NOTES

System reset for lithium battery back-up SA56600-42

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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